JEDEC Board Drop Test Simulation for Wafer Level Packages (WLPs)

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Abstract

In this paper, a comprehensive study is carried out to investigate the WLP package dynamic behaviors subjected to drop impact according to the JEDEC specification. First, a Direct Acceleration Input (DAI) method, which decouples the board dynamic responses from the test system, thus avoids the difficulties in modeling the complex behaviors of contact between the drop table and drop surfaces, is introduced. The equivalency of the DAI and Input-G methods has been proved mathematically and numerically in this paper. The DAI method removes a rigid-body motion of a test board. Second, the accuracy of global/local modeling techniques is examined in details. Very consistent results were obtained with various distances of cut boundary ranging from 1.5mm to 3.0 mm for the extended PCB board dimension from the package edge. Third, the dynamic responses of each component on JEDEC board are investigated. It is found that for WLP, the component U1, which is the closest to the mounting hole, will fail first due to the local bending effect. This is different from BGA packages. Such results have been validated by recently reported test data. It is noted that the crack initiation of solder ball always starts at the inner side. The corner balls at each component will fail first compared to the balls in other locations on the same components. The maximum peel stress contours for those critical corner balls at each component map the actual solder ball cracks very well. Fourth, the correlation of the board strain to the solder ball stress is studied with different package sizes with or without underfill. It is observed that board strain at the corner locations of component are not always proportional to the damage exerted on solder balls. Therefore caution must be taken when board strain alone is used to evaluate package dynamic performance. Finally, an improved JEDEC board design is proposed to avoid early failure of corner components by moving the screw locations further away from the current specified location. The components at the center column of the modified board will fail first, as observed in many BGA packages. The new board design ensures the package failures come from package intrinsic designs.

1. Introduction

Wafer level packaging (WLP) is gaining tremendous interest throughout the semiconductor industry, due to the rapid advances in integrated circuit fabrication and the demands of an emerging market for smaller, thinner, and faster, yet less expensive electronic products [1-3]. Wafer-level packaging paves the way for true integration of wafer fab, packaging, test, and burn-in at wafer level, for the ultimate streamlining of the manufacturing process undergone by a device from silicon start to customer shipment. The handheld electronics industry is quickly realizing the benefits of switching from a traditional leadframe package to a WLP because it provides the small form factor to satisfy multifunctional device requirements along with improved signal propagation for optimum performance. New products designed in the front end for WLP applications are smaller than their wirebond counterparts. Overall, WLP enables the next generation of portable electronics at a lower cost.

The mechanical shock resulted from mishandling during transportation or customer usage may cause the bare-die bumped package solder joints failure, which leads to malfunction of product. Normally, mobile phones are designed to withstand certain accidental drops to the floor from a certain height, without causing major mechanical or functional failures. Over the past few years, there is an increasing research interest in drop test and simulation, due to higher industrial demand [4-10]. The JEDEC has published a test standard with detailed test procedures and board design for board level drop test of components used in handheld electronic products [4]. Since board level drop test is a key qualification test for portable electronic products, it is becoming a topic of great interest by many researchers. Numerous works on drop test experiments and simulation were reported over the past few years.

In this paper, a comprehensive numerical study is carried out to investigate the WLP package behaviors subjected to drop impact according to the JEDEC specification. First, a Direct Acceleration Input (DAI) method is introduced, which decouples the board dynamic responses from the test system, thus avoids the difficulties in modeling the complex behaviors of contact between the drop table and drop surfaces. The equivalency of the DAI and Input-G methods has been proved mathematically and numerically. Second, the accuracy of global/local modeling techniques is examined in details. The effect of cut boundary distance and different local model structures are investigated. Third, the dynamic responses of each component on JEDEC board are studied carefully. Crack propagation pattern of each solder ball for different components on JEDEC board is examined. Fourth, the correlation of the board strain to the solder ball peeling stress is studied for different package sizes and with or without underfill. Finally, an improved JEDEC board design is recommended to avoid early failure of corner components of a WLP package. The new board design ensures the package failures come from package intrinsic designs.

2. Direct Acceleration Input (DAI) Method

Due to demand for short time-to-market, drop testing has become a bottleneck for semiconductor and tele-communication industry. Therefore, there is a need for a faster and cheaper solution, i.e. validated drop impact model, which is accurate, reliable, and enables understanding of physics-of-failure for design improvement. Several modeling methods

have been developed to satisfy the requirements in package design analysis [10].Various advanced drop test modeling techniques have been developed for various applications, consisting of analysis type (dynamic vs. static), loading method (free-fall vs. input-G), and solver algorithm (explicit vs. implicit). In the so-called Input-G method, the drop table, fixture, contact surface, and friction of guiding rods in drop test setup are not needed to simulate, but their complex effects are considered indirectly by using the an impact pulse subjected to the board mounting holes. The problem is therefore formulated mathematically as follows,

$$[M][\ddot{u}_1] + [C][\dot{u}_1] + [K][u_1] = 0 \tag{1}$$

with initial conditions

$$[u_1]\Big|_{t=0} = 0 \quad , \qquad [\dot{u}_1]\Big|_{t=0} = \sqrt{2gH} \tag{2}$$

and boundary condition

$$a = \begin{Bmatrix} 1500g\sin\dfrac{\pi t}{t_w} & \text{for } t \le t_w, \quad t_w = 0.5 \\ 0 & \text{for } t \ge t_w \end{Bmatrix} \tag{3}$$

where the equation (3) is based on the JEDEC specification for the drop table acceleration profile, with a peak value of the acceleration of 1500g and the impulse duration as 0.5ms, and no-rebound taking place. $[M]$ is the mass matrix, $[\ddot{u}_1]$ is the acceleration, $[C]$ is the damping matrix, $[\dot{u}_1]$ is the velocity, $[K]$ is the stiffness matrix , g is acceleration due to gravity, $[u_1]$ is the displacement and t is time after impact.

It is noted that most commercial finite element software does not provide acceleration at the surface for loading input. Therefore, some special treatment must be carried out to correctly apply the loads to the board. Large mass method, in which a large mass is attached at the point where the acceleration input is given, can converted the acceleration input into force input by multiplying the acceleration with the large mass [9]. Alternatively, equation (3) can be integrated to become a displacement boundary condition as follows.

$$[u_1]\Big|_{at\,hole} = \begin{Bmatrix} -\left(\dfrac{t_w}{\pi}\right)^2 (1500g)\sin\dfrac{\pi t}{t_w} + \left(\dfrac{t_w}{\pi}(1500g) + \sqrt{2gH}\right)t, & t \le t_w \\ \left(2\dfrac{t_w}{\pi}(1500g) + \sqrt{2gH}\right)t - \left(\dfrac{t_w}{\pi}\right)^2 (1500g), & t \ge t_w \end{Bmatrix} \tag{4}$$

This method is called input-D (displacement) method. It should be noted that when equation (3) or (4) is applied, the board response includes a rigid body movement. In other words, the board displacements will be infinite with time increasing.

The direct acceleration input (DAI) method was introduced [6] as an alternative to input the dynamic loading while removing the rigid body motion. In this method an acceleration impulse is applied as a body force to the problem under study. The surfaces of mounting holes are fixed during dynamic responses. Therefore, the problem formulation becomes

$$[M][\ddot{u}_2] + [C][\dot{u}_2] + [K][u_2] = \begin{Bmatrix} -[M]1500g\sin\dfrac{\pi t}{t_w} & t \le t_w, t_w = 0.5 \\ 0 & t \ge t_w \end{Bmatrix} \tag{5}$$

with initial conditions

$$[u_1]\Big|_{t=0} = 0 \quad , \qquad [\dot{u}_1]\Big|_{t=0} = \sqrt{2gH} \tag{6}$$

and boundary conditions

$$[u_2]\Big|_{at\,hole} = 0 \tag{7}$$

The above equations have been proved analytically to be equivalent to the original problem formulations in equations (1)-(3), except a difference of a rigid body movement [8]. This means,

$$\begin{aligned} [u_2] &= [u_1] - [u_1]\Big|_{at\,hole} \\ [\dot{u}_2] &= [\dot{u}_1] - [\dot{u}_1]\Big|_{at\,hole} \\ [\ddot{u}_2] &= [\ddot{u}_1] - [\ddot{u}_1]_{at\,hole} \end{aligned} \tag{8}$$

With DAI, the loading input becomes easier and more straightforward, such as in ANSYS. In order to further confirm the equivalency of the DAI with the original problem, the simulation of a JEDEC drop test board with WLP components is carried using both large mass and direct acceleration methods. Due to the symmetry, a quarter finite element model (66mm × 38.5mm × 1mm) of a JEDEC board is developed. Figure 1 shows a schematic of lower left quarter part of the test board with six components U1, U2, U3, U6, U7 and U8, which are numbered according to the JEDEC standard. The line AB is defined across the board with a distance of 1 mm away from edges of components U1, U2 and U3. Figure 2 plots the board strain for a 6mm×6mm chip size model in x direction along the line AB at the time of 1.5 ms using both methods. It is seen that same results were obtained. This implies that the two loading methods are equivalent.

As discussed earlier that, the displacement will be different for the two methods since with the DCA, the board vibrates while hole locations are fixed. For input-G method, the board will move forth continuously along z direction while board is vibrating. Figure 3 shows the acceleration time history graph using two methods. The location is at the top of component U8 (see Figure 1). It is seen from this figure that the acceleration solutions have different values for the initial 0.5 ms acceleration impulse period. However, after this period they overlap. The difference between these two curves is exactly the half-sine acceleration impulse, as expected from the analysis.

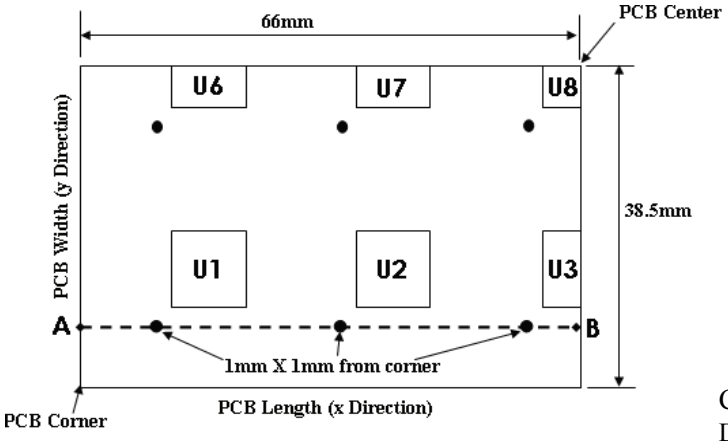


Figure 1 Schematic of Lower Left Quarter Part of Test Board

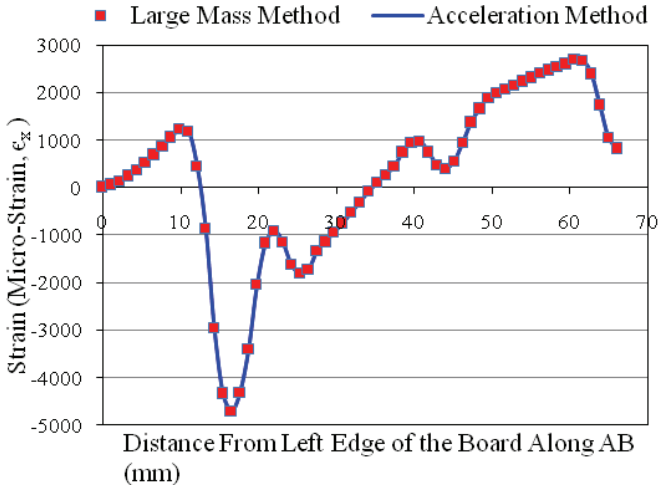


Figure 2 Strain Distribution Comparison with Two Methods (along the line AB at t = 1.5 ms)

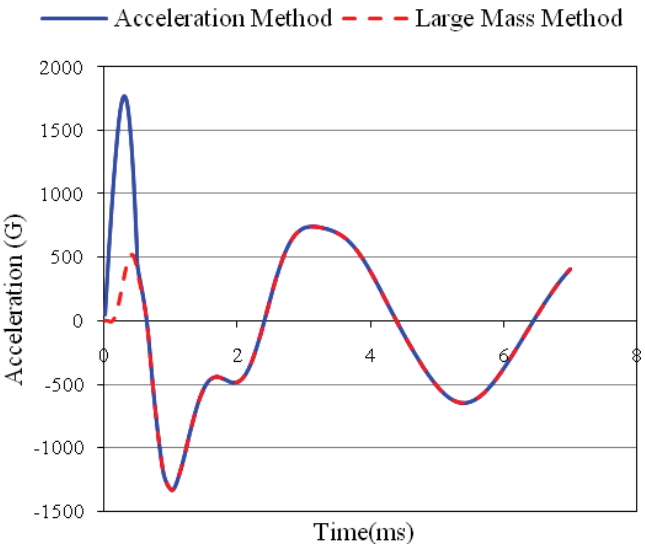


Figure 3 Acceleration Time History Comparison using Two Methods.

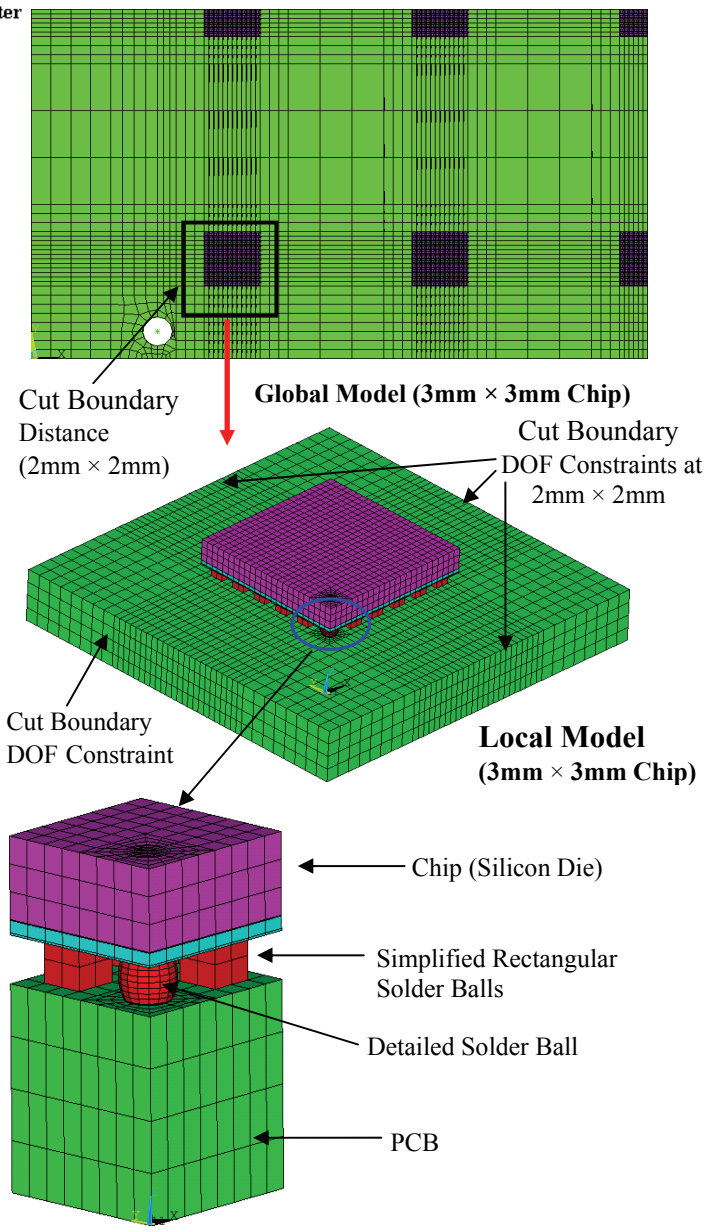


Figure 4 Global/Local Modeling Technique on a 3mm ×3mm Chip Quarter Section Model

3. Accuracy of Global/Local Modeling

The main failure mechanism under impact loading for a WLP is solder ball cracking. There are 15 components on a JEDEC board, and each component has hundreds of solder balls. It becomes obvious that the FEA model becomes too big to be handled without global/local modeling or submodeling technique applied. Figure 4 shows a diagram for the process of global/local modeling of a test board with a 0.5mm solder ball pitch for a 3mm×3mm chip size wafer level package. In the global model, each solder ball is simplified as a cubical block with one element only. The local model can be placed at any component location with an extended PCB dimension. Figure 4 shows an example of the local model at component U1 location. In this case PCB boundaries are cut around the chip at a distance of 2mm × 2mm from the edge of

the chip. In the local model, the detailed WLP structure can be modeled in details. Two different local models are built for analysis. Figures 5 and 6 show two different local models, i.e., namely, detailed solder ball model (Local Model 1) and rectangular solder ball model (Local Model 2) respectively. In the detailed solder ball model all solder balls are modeled with detailed structures, while in the rectangular solder ball model refined meshes are made on the critical corner solder ball only. All other solder balls are modeled as rectangular blocks. The detailed solder ball model has 90,808 nodes and 72,928 elements, while the rectangular solder ball model has 9,936 nodes and 9,823 elements only for a 3mm×3mm chip size and 0.5mm solder ball pitch WLP local model.

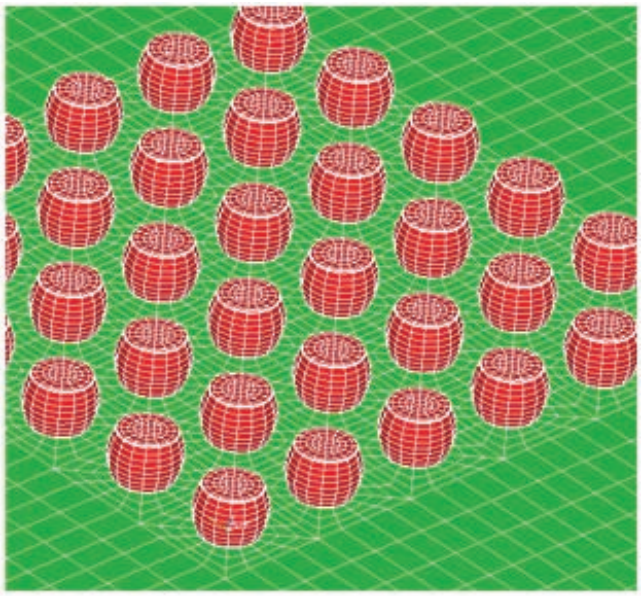


Figure 5 Detailed Solder Ball Local Model (Local Model 1)

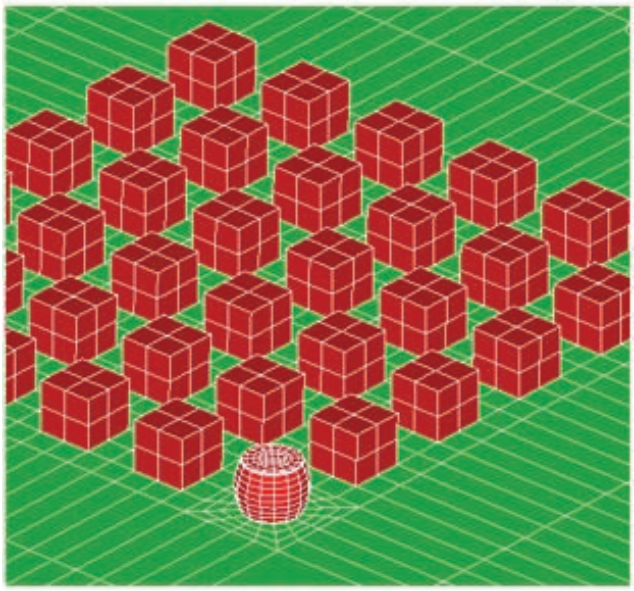


Figure 6 Rectangular Solder Ball Local Model (Local Model 2)

One of the concerns using global/local modeling is the accuracy of results. It is important to know if the cut boundary is far enough from the local interested location. Four cut boundary distances of 1mm × 1mm, 1.5mm × 1.5mm, 2mm × 2mm and 2.5mm × 2.5mm from the edge of the component are simulated. Figure 7 shows the maximum peel stress for the four different cut boundary conditions at component U1. It is seen that the difference is less than 4%. This implies that a local model with a cut boundary distance of 2mm × 2mm can give accurate results on local stresses in solder balls.

Figure 7 Effect of Cut Boundary Distance in Global/Local Modeling

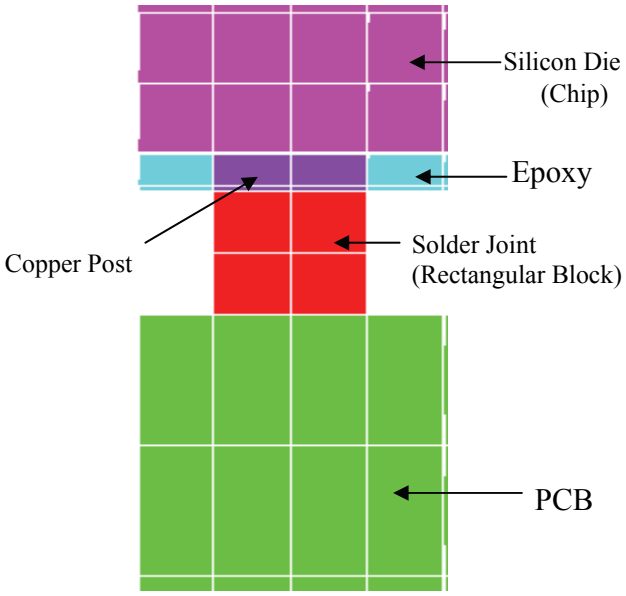


Figure 8 Details of FE Rectangular Ball

Figure 8 shows a cross-section view of a finite element model for a rectangular solder ball local model. This model includes other details such as copper post, epoxy and passivation in order to match the mesh pattern and connect smoothly to the refined solder ball region. Figure 9 is the cross-section view of a refined finite element mesh pattern for

a critical solder ball. Since the failure is often at the intermetallic layer or between intermetallic layers [10], a 10 µm intermetallic layer with two layers of mesh is modeled at solder/copper post interface. The material properties used for the local and global finite element models are listed in Table 1. All the materials are considered as linear elastic models. The PCB is considered as a damping material. The coefficient of damping is calibrated through experimental data.

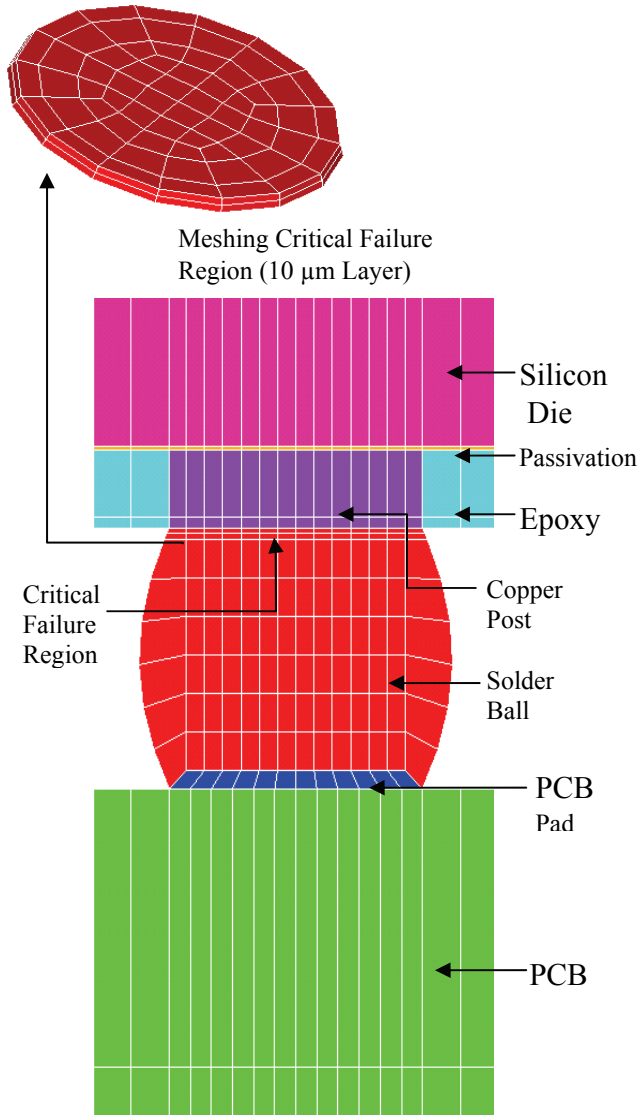


Figure 9 Details of FE Detailed Solder Ball

Both local models are used to extract solder stress state for component U1 and U8. Figures 10 and 11 show the results of peel stress at corner solder balls for components U1 and U8 respectively. The difference between the two models is less 6%. The rectangular solder ball model presents a significant computational savings without sacrificing the accuracy.

Table 1. Material Properties for Global and Local FE Models

Material	Mechanical Properties			Typical Dimensions
	Modulus (GPa)	Poisson Ratio	Density (gm/cm^3)	
PCB	22	0.25	2.1	132mm × 66mm × 1mm
Solder (SAC)	51	0.36	7.2	Diameter, 310 × 10^{-3} mm
Silicon Die	130	0.278	2.5	Thickness, 400 × 10^{-3} mm
Underfill	10	0.3	2.0	Thickness, 234 × 10^{-3}mm
Copper Post	128.8	0.34	8.3	Thickness, 70 ×10^{-3} mm
Epoxy	4.7	0.38	2.2	Thickness, 70 × 10^{-3} mm
Passivation	2.89	0.34	2.2	Thickness 4 ×10^{-3} mm
PCB Pad	128.8	0.34	8.3	Thickness 17 × 10^{-3} mm

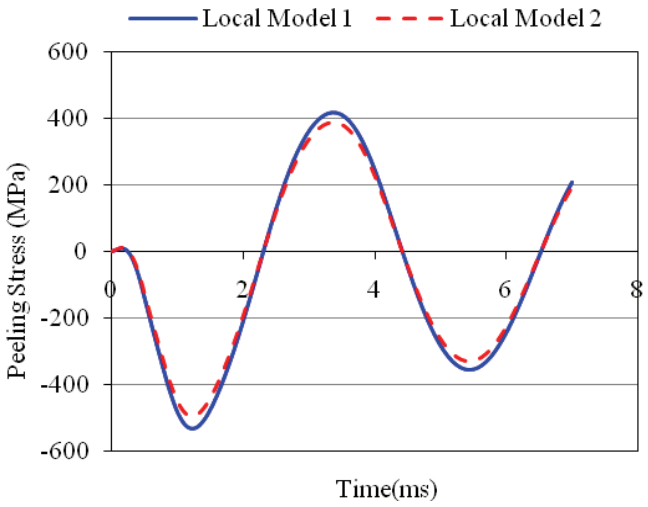


Figure 10 Peeling Stress Time History Comparison of Local Model 1 and Local Model 2 for Component U1

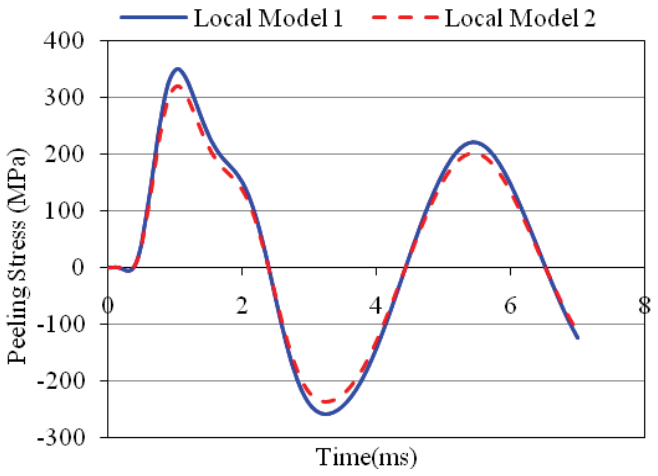


Figure 11 Peeling Stress Time History Comparison of Local Model 1 and Local Model 2 for Component U8

4. Dynamic Responses of Individual Components on JEDEC Board

Figure 12 shows the maximum peel stresses developed in all components of a quarter test board under impact. Figure 13 shows the peel stress time history plot for all components. It is noted from these figures that the stress developed in component U1, which is nearest to the mounting hole, is the highest among all components. The stress developed in component U8 is slightly less than component U1. Overall, the stress developed in components can be ranked as: U1>U8>U3>U2>U7>U6. Such results are different from a BGA package [9], in which the most critical component is U8 or U3. The simulation results shown in Figure 12 and Figure 13 are confirmed with experimental data reported in the paper [11, 12].

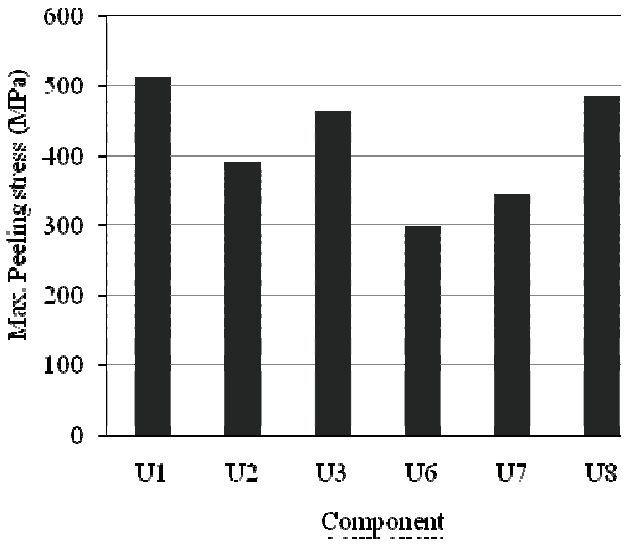


Figure 12 Maximum Peeling Stress in Components

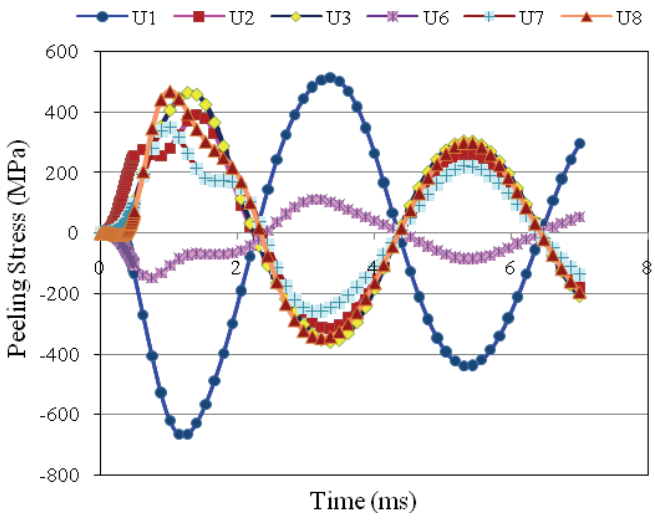


Figure 13 Maximum Stress Time History Plot in Components

Figure 14 shows the stress contour plots of each corner ball of the component U1. It is observed from this figure that the maximum stresses of all corner balls are developed from the inner side regions (towards the component center). It can be concluded from this observation that the crack would initiate inner side of each solder joint and propagate diagonally. Similarly, stress contours for all other components are shown in Figure 15.

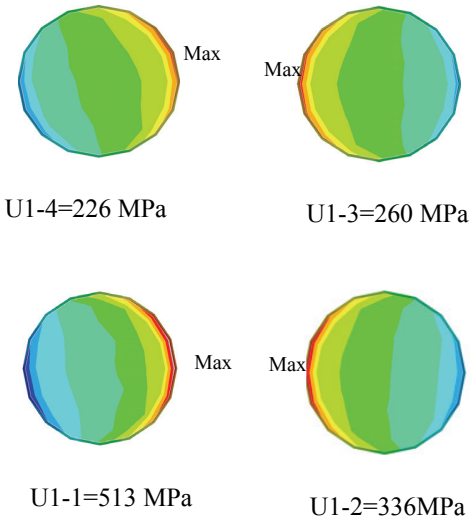


Figure 14 Stress Contour Plots for Component U1 (4 Corner Balls)

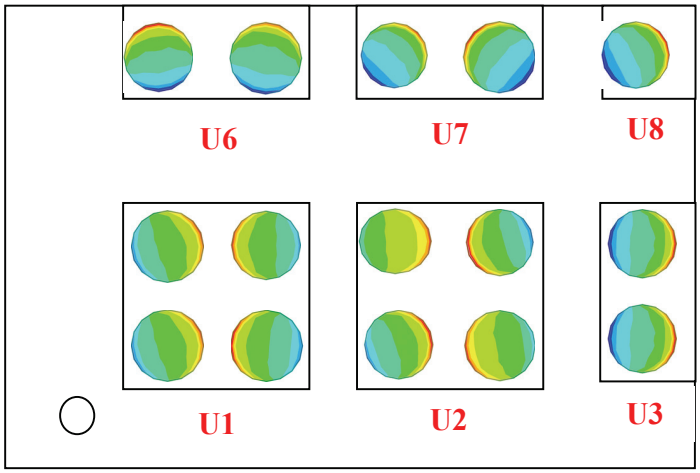


Figure 15 Stress Contour Plots for All Corner Balls of All Components

5. Correlation between Board Strain and Solder Ball Stress

Since it is impossible to measure the stresses and strains in solder balls, strain measurement at PCB at various locations has been considered as a metric to evaluate the stress kevel in solder balls. It has been commonly recognized that the board strain at the location near the package corner would determine the limit of PCB loading, regardless of package types and loading conditions. In this section, the results for different sizes of WLPs with and without underfill will be examined to

show that the correlation between board strain and solder ball stress virtually do not exist.

Figure 16 shows the comparison of peak corner strain calculated on PCB component side at 1mm×1mm distance away from component corner (see Figure 1) with the maximum peel stress developed in solder balls for 6 components. Maximum board strain in x direction is used in comparison. While, overall the higher corner board strain will induce higher stress in solder ball, the exact correlation is not evident. This implies that using board strain alone as a metric for solder joint performance is not sufficient.

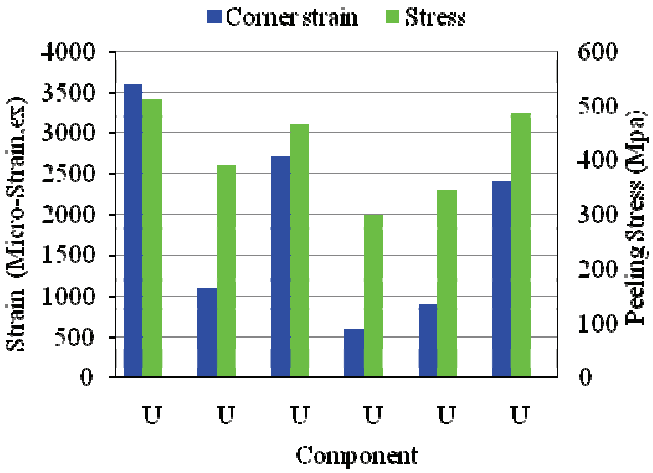


Figure 16 Comparison of Board Strain and Solder Joint Stress

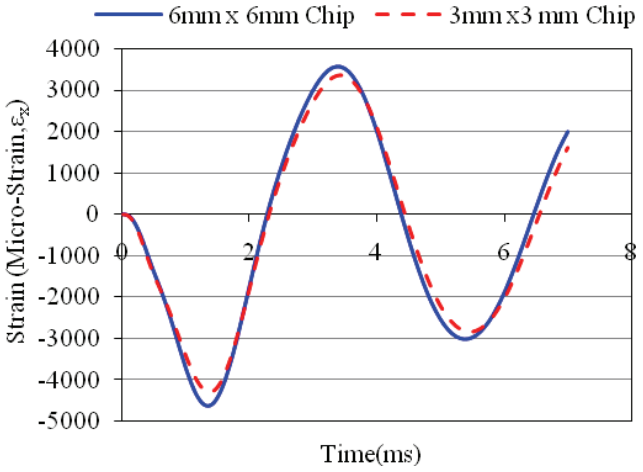


Figure 17 Strain Time History Comparison of Different Size Packages for Component U1

Further, the test board is analyzed for two different chip sizes, 3mm×3mm and 6mm×6mm, respectively. The board strains (component side) and stresses in solder joints are calculated, respectively. Figure 17 shows the graph for strain time history comparison of component U1 for the two different packages. The strain increases slightly with chip size increasing.

The maximum peel stresses for components U1 and U8 for both package sizes are shown in Figure 18. The stress in the solder joint increases significantly with package size increasing. Experimental data confirmed that the 6x6mm WLP solder joints failed much earlier for 3x3 WLP [12]. However, the board strains for these two WLP options are approximately the same. This again suggests that the caution must be taken when the board strain is used as a metric for solder joint performance under impact loading.

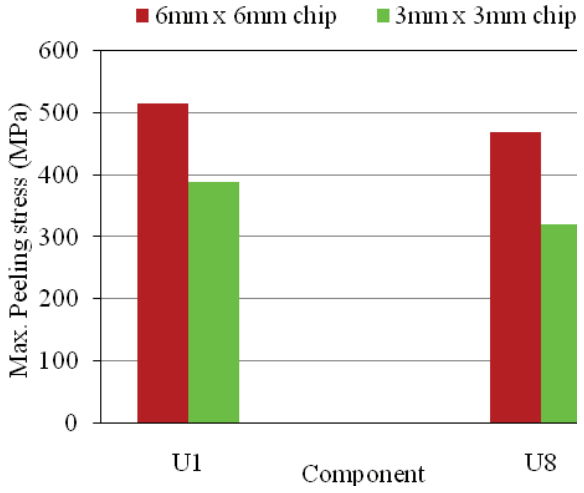


Figure 18 Maximum Peel Stress Comparison of Different Size Packages for Components U1 and U8

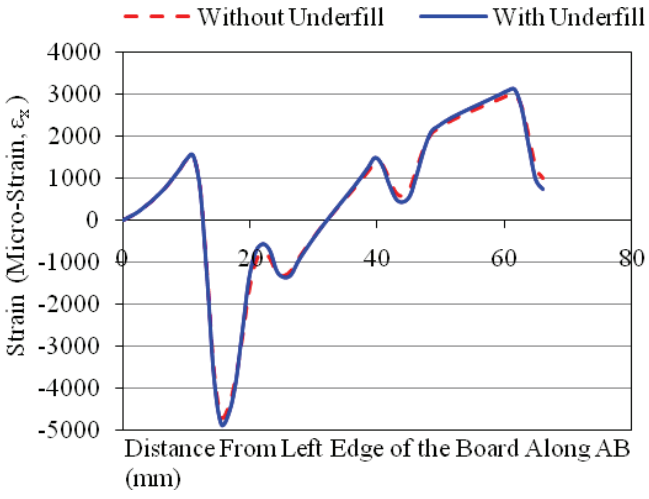


Figure 19 Effect of Underfill on Board Strain Distribution in x Direction Along Line AB at t = 1.5 ms

The correlation between board strain and solder ball stress can be further demonstrated through the effect of underfill. A 6mm × 6mm chip size component is used for this purpose. The board strain ε_x, calculated at time of 1.5ms along path AB (see Figure 1), is shown in Figure 19. It is seen from this figure that there is no significant change in the strain value for the two cases with and without underfill.

To study the effect of underfill on solder joints stress the modeling is performed with 3mm×3mm and 6mm× 6mm chip size packages, respectively. The maximum peel stress is

calculated at U1 and U8 for both packages. Figure 20 shows the plot for the maximum peel stress for two packages with and without underfill. There is a significant reduction (more than 70%) in the solder joint stress in the presence of underfill. It is apparent that the board strain is not able to capture such an effect. Additional investigations have been conducted on the board strain at locations right beaneth the solder balls. Board strain at these locations indeed capture the trend in solder joint stress but the strain reduction is shwon to be much less than stress reduction.

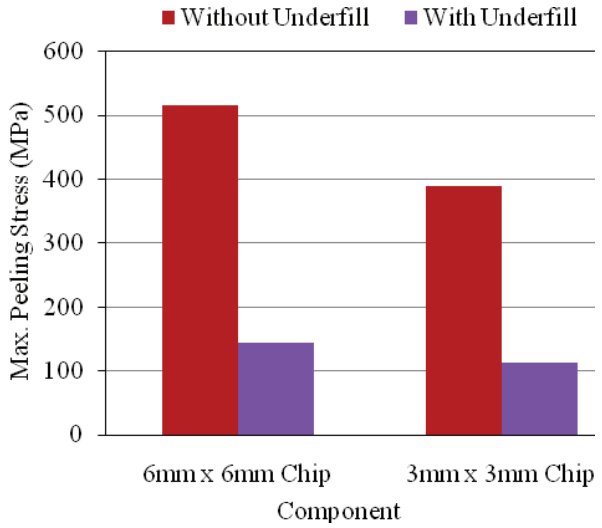


Figure 20 Maximum Peeling Stress Comparison with and without Underfill at U1

6. Improved JEDEC Board Design

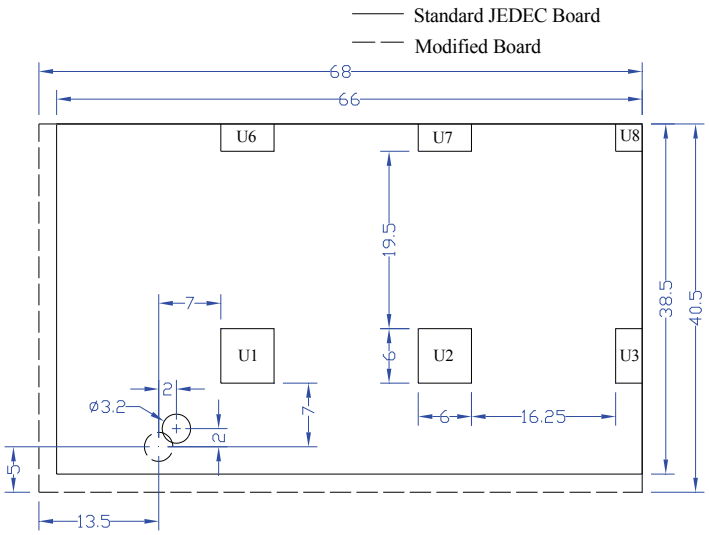
It is known from the earlier investigations that WLP components, which are placed near the mounting holes on JEDEC test board, experience the highest level of stresses in solder joints, therefore, would fail first during drop test. Such observations have not been found in BGA packages. It is important to note that this failure is due to the local bending effect applied due to the mounting hole constraints. In other words, the corner components failures are not caused by the intrinsic factors of WLP package design. In the following discussion, some modifications to existing JEDEC board are made and the new results will shed light to the failure mechanisms of corner components.

According to the current JEDEC board design specification, the mounting hole center is set with a distance of 5mmx5mm from the package corner, regardless of package sizes. In this study, a modified board design is made, which extends the whole board dimension by 4mm × 4mm in length and width directions, such that the mounting hole center will be moved further away from the package corner by an additional 2mmx2mm. The distance between the mounting hole to package corner is 7mmx7mm for the modified board. Figure 21 shows the modified board design. All other geometries remain same.

A 3mm×3mm chip size model is used for both boards. Figure 22 shows the board strain at package corner of component U1 for the two models. It is noted from the figure that board strain decreases significantly for the modified board at U1.

Figure 23 shows the stress time history for standard board and modified board for component U1. It is noted from this figure that there is a significant decrease in stress value for the modified board at component U1.

Figure 24 shows the maximum peel stress in solder balls for all components with standard and modified board designs. There is a significant decrease (more than 30%) in the stress value for modified board at U1, while stresses in other components have trivial changes. Therefore, it is evident from this observation that mounting holes have significant effect on the performance of components nearest to them. This suggests that the failure of components located near mounting cannot be considered as the criteria to measure the reliability of a WLP package.



Note: All Dimensions are in mm

Figure 21 Schematic of Lower left Quarter Part of Standard JEDEC Board and Modified Board

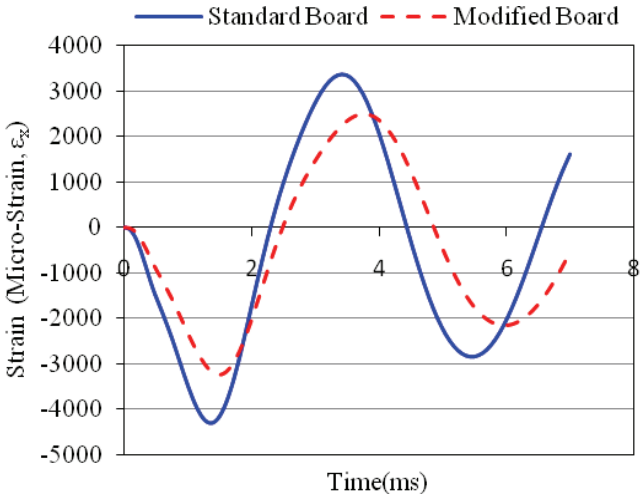


Figure 22 Strain Time History Comparison of Standard JEDEC Board and Modified Board at U1

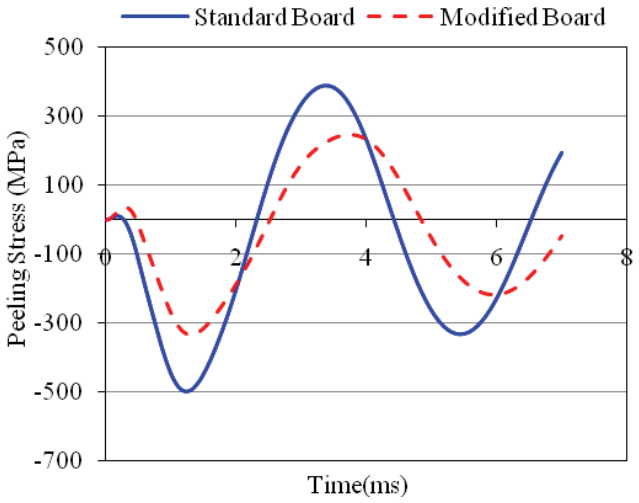


Figure 23 Stress Time History Comparison of Standard JEDEC Board and Modified Board at U1

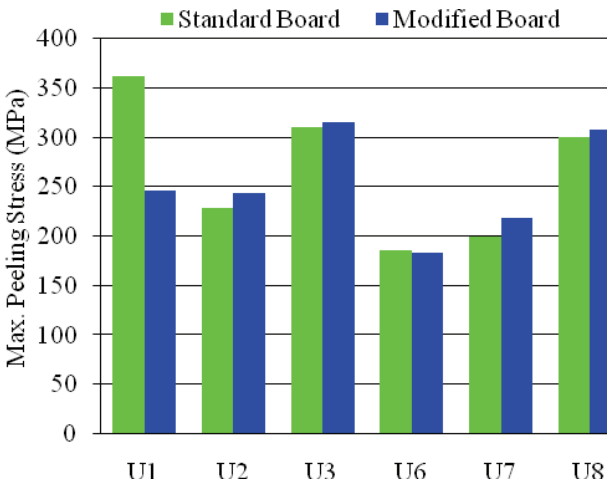


Figure 24 Maximum Peeling Stress Comparison of Standard JEDEC Board and Modified Board

Conclusions

The finite element modeling of dynamic behaviors of wafer level packages under impact loading has been performed. The JEDEC/ JESD22-B111drop test board with Cu post WLP packages were modeled. This paper presented a mathematical proof of the equivalency of the direct acceleration input (DAI) method with the input-G or input-D method. Numerical results validated the analytical proof.

The effect of the cut boundary distance in global/local modeling was investigated. Very consistent results were obtained with various distances of cut boundary ranging from 1.5mm to 3.0 mm the extended PCB board from the package edge. It is suggested that the use of a cut boundary distance of 2mm×2mm away from the package corner presents satisfactory results.

Local peel stress at IMC layer can be extracted from a local model analysis, and the rank can be made as U1>U8>U3>U2>U7>U6. This implies that the component U1, which is located mostly closely to the mounting hole, fails first. Such results are different from those test results reported in literature on BGA packages. This implies that a WLP failure mechanism might be different from BGA packages.

The stress contour plot for solder joints showed that the crack propagation always from inside package to outside, which are supported by the experimental data.

The correlation between board strain and solder ball stress is demonstrated through two examples of package size effect and underfill effect. Both results showed that board strain is not able to capture the change of solder joint stress when package size changes or when underfill is used. The caution must be made to use the board strain as a metric to evaluate the solder joint performance under impact loading.

An improved JEDEC board design is suggested to avoid early failure of corner components by moving the mounting hole further away from the current specification. The components at the center column of the modified board would fail first, as observed in many BGA packages. The new board design ensures that the drop test failures are due to package intrinsic strength rather than effect of mounting screws.

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