Wafer Level System Packaging and Integration for Solid State Lighting (SSL)

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Abstract
In this paper, wafer level system packaging and integration for solid state lighting (SSL) is presented, which includes wafer level phosphor coating, wafer level LED chip encapsulation, wafer level optics manufacturing, reconfiguration (or reconstitution) of LED/silicon wafers, through silicon vias (TSV) formations between LED and silicon/ceramics/polymer wafers, wafer-to-wafer or wafer-to-chip bonding and stacking, and wafer level bumping technologies. A variety of wafer level bumping technologies is introduced, such as ball-on-I/O (BON), ball on polymer (BOP), redistribution dielectric layer (RDL) process, and copper post bumping process. The reliability improvement among different bumping technologies and the implications in SSL systems are discussed.

1. Introduction
Light emitting diode (LED) is a solid-state lighting (SSL) source that converts electricity directly into light. SSL provides high energy efficiency in lower power consumption, longer life, and higher performance. Because of this, general lighting and illumination is now going through a radical transformation from traditional incandescent bulbs and fluorescent lamps to SSL based illumination systems [1].

A solid state lighting (SSL) system is usually composed of the following subsystems: LED lighting sources (packaged LED or LED module/emitter), thermal management designs (e.g. fans and heat sinks), driver and control electronics, and optics. Most of LEDs today are packaged on an individual component basis. Figure 1 is a schematic illustration of current LED chip packaging process. LED wafer is diced into individual LED chips before packaging. The packaging process includes silicon submount (by flip chip or wire bond), phosphor coating, epoxy encapsulation, lens attachment, heat sink and outer package assembly, as illustrated in Figure 2. Such a component level packaging process has a relatively low throughput. Consequently it is more difficult to implement automation for large scale mass production, which is a critical element for low cost manufacturing. Therefore, a more efficient packaging process at wafer level in batch process is in demand in the LED industry.

In this paper, a general overview of wafer level system integration is presented. Then wafer level LED chip packaging, including: wafer level phosphor coating, wafer level encapsulation and wafer level optics, is discussed. A variety of wafer bonding and stacking technologies is introduced. Finally wafer level bumping technologies are described, with an emphasis on thermomechanical reliability considerations. New interconnect technologies such as hollow solder balls and polymer core balls are also introduced concerning reliability enhancement.

2. Overview of SSL System Integration
In a typical SSL system, the packaged LED module (or emitter) must work with other components, such as application specific integrated circuits (ASIC), LED driver, sensor, radio frequency (RF) circuit, power controller, processor, or memory, and additional heat dissipation component etc. There is a potential breakthrough and technology development for 3D system integration for SSL systems. Tsou et al. attempted to demonstrate a silicon-based packaging platform for wafer level LED packaging using silicon bulk micromachining technology [2]. Lim et al. developed a wafer level encapsulation process for LED packages [3]. Zhang and Lee developed a deep reactive ion etching (DRIE) trenches based LED wafer level packaging process [4, 5]. For wafer level LED chip packaging, the corresponding equipment is also made available, for example, for wafer level phosphor coating and wafer level optics process [6].
Lau et al. [7] envisioned a concept of full 3D SSL integration using through silicon via (TSV) and wafer-level bonding and stacking technologies. Figure 3 is a schematic conceptual illustration of such an integrated SSL system [7]. The passive Si submount in a LED module is replaced by an IC chip such as the ASIC, LED driver, processor, power controller, sensor, RF, etc., i.e. integrating the LEDs and the IC chip together in a 3D manner. Their electrical feed-through and some of the thermal paths can be effectively achieved by the through silicon vias (TSV) filled with copper w/o redistribution layers (RDL) on the IC chip. The integrated device is assembled using wafer level bumping technology. The active IC chip can be used to support the multi-LEDs for many functions, e.g. dimming and lighting control, step-up and step-down topologies, power conversion, electrical feed-through, and thermal management.

3. Wafer Level LED Chip Packaging

Wafer level LED chip packaging consists of wafer level phosphor coating, wafer level encapsulation, wafer level optics, and LED wafer reconfiguration. Figure 4 describes a wafer level encapsulation process, developed by Lim et al. [3]. As illustrated in Figure 4, a high viscous photoresist is patterned on wafer and reflowed into dome-shape islands. The Nickle plating process is then performed on wafer to form a mold. Subsequently, a UV curable polymer is dispensed onto the Ni mold and is cured to form a whole piece of encapsulation array. The encapsulation array can then be attached onto a wafer on which LED arrays are mounted. In this manner a wafer level LED packaging process is realized.

Zhang and Lee developed a DRIE trenches based LED wafer level packaging process [4]. A 4-inch p-type wafer serves as the substrate for LED arrays. The fabrication of the wafer substrate is made by micro fabrication and wafer level plating process.

Figure 5 shows the wafer level phosphor coating by spray coating of diluted phosphor solutions on processed LED wafers [6]. The advantages of such a process are: 1) high coating uniformity of topside and sidewalls of the dies; 2) low phosphor consumption; 3) easy solution-based tuning of the color temperature and color rendering index; 4) fast batch processing on wafer-level; 5) reduced binning; and 6) multiple remote phosphor layers possible.
To perform wafer level optics and wafer level phosphor coating, the LED wafer needs to be reconfigured. Figure 6 shows a typical process of wafer reconstitution (or reconfiguration) [8-10]. The “good tested” LED dies are placed face-down onto a carrier with an adhesive tape. The distance (pitch) between the dies on the carrier defines the fan-out area around the chips and is freely selectable. The carrier with the adhesive tape holds the dies in position and protects the active side of the dice during molding. A mold compound is used to combine the placed LED dies to wafer format in compression mold technique. After this, the reconstituted wafer is released from the carrier system, which can be re-used afterwards. Wafer reconfiguration is one of critical processes in fan-out wafer level packaging.

Figure 6 A typical process of wafer reconstitution (or reconfiguration) of LED dies

4. TSV Process and 3D LED and IC Packaging Integration

Many new developments are currently underway to incorporate 3-D packaging technology with WLP solutions into SSL systems for a full integration realization. TSV technology has been one of key elements in 3D integration. The main advantage of the TSV technology with WLP is to reduce the size of the device module. Three-dimensional integrated circuits (3D IC) has been generally acknowledged as the next generation semiconductor technology with the advantages of small form factor, high-performance, low power consumption, and high density integration. TSV and stacked bonding are the core technologies to perform vertical interconnect for 3D integration. For the fabrication approach, there are three stacking schemes in 3D integration: chip-to-chip, chip-to-wafer, and wafer-to-wafer. Wafer-to-wafer technology can be applied for homogeneous integration of high yielding devices. Wafer-to-wafer bonding maximizes the throughput, simplifies the process flow, and minimizes cost. The drawback for this wafer-to-wafer method is the number of known-good-die (KGD) combinations in the stacked wafers will not be maximized when the device wafer yields are not high enough or not stable. In this case, chip-to-chip or chip-to-wafer will be adopted to ensure vertical integration with only good dies. Considering mass production in future, the chip-to-wafer and wafer-to-wafer technologies have gradually become the mainstream for 3D integration.

Wafer bonding and stacking technologies can be further differentiated by the method used to create TSVs: either via-first or via-last. The common definition for via-first and via-last is based on TSVs formed before and after BEOL process. TSV fabrication after the wafers are bonded, using a “drill and fill” sequence, is definitely via-last approach. Whereas via-first and pre-bonding via-last approaches, building TSVs on each wafer prior to the bonding process are generally more efficient and cost-effective. The leading wafer-level bonding techniques used in 3D integration include adhesive bonding (polymer bonding), metal diffusion bonding, eutectic bonding, and silicon direct bonding.

5. Wafer Bumping and Reliability Considerations

Wafer bumping is one of the most important assembly steps in wafer level packaging and integration. Since there exists an intrinsic difference in the coefficient of thermal expansion (CTE) between LED/silicon wafers (~2.6ppm/°C) and PCB (~17ppm/°C), solder ball reliability under thermal cycling loading is apparently limited by die-size [11, 12]. The larger the die size is, the greater thermal stresses are developed at the outmost solder balls due to the effect of distance from neutral point (DNP). To improve solder ball reliability performance, several bumping technologies have been developed, such as ball on nitride (BON) [13], ball on polymer (BOP) [14, 15], and copper post WLP [16].

To understand the mechanism of reliability for various bump structures, finite element modeling is performed to investigate the accumulated inelastic strain energy density at solder ball/chip region subjected to -40°C and 125°C thermal cycling [12]. Figure 7 plots the per-cycle inelastic strain energy densities for the four fan-in WLP structures, for a 12x12 array package with 0.5mm pitch. It can be seen that, compared to the ball on nitride structure, all other three structures: BOP without UBM, BOP with UBM, and copper post WLP, show more than 30% reduction in terms of the accumulated inelastic strain energy density per cycle. This means that, with the incorporation of a dielectric polymer film or an encapsulated copper post layer embedded in an epoxy, between solder balls and chip, the stresses in solder joints can be reduced significantly compared to a ‘rigid’ ball connection as in a BON configuration.

For ball on polymer structures, the extreme compliance of the polymer film is attributed to be the reason for thermal-mechanical performance improvement in solder joints. The Young’s modulus of polyimide film is 1.2GPa, which is one order lower than the modulus of solder alloy (50GPa for SAC305). The polymer film creates a ‘cushion’ effect to reduce the stresses transmitted to solder joints. Studies have shown that the coefficient of thermal expansion (CTE) of the polymer
film has insignificant effect on solder joint stresses provided that the polymer film modulus is extremely low.

Fan-out WLPs are structurally similar to the conventional ball grid array (BGA) packages, but eliminate expensive substrate processes. The critical solder balls in a fan-out WLP are located beneath silicon chip area, where the maximum CTE mismatch occurs between the silicon chip and PCB [12].

To improve the compliance of WLP structures, solder balls may be constructed with nano-size column like or honeycomb like structures [17]. Some possible configurations of ‘hollow solder balls’ are illustrated in Figure 9. These new ball structures would need new process to realize. The rapid advances in nano-material and nano-manufacturing developments would make it happen in the near future. The ‘ball’ materials are not limited to ‘solder alloys’.

![Inelastic strain energy density for different bump structures](image)

Figure 7 Inelastic strain energy density for different bump structures: A. BON; B. BOP without UBM; C. BOP with UBM; and D. Copper post [10].

On the other hand, for copper post WLP structure, the beneficial effect comes from the larger CTE of copper post and epoxy, which are typically 17×10⁻⁶/°C and 20×10⁻⁶/°C, respectively. The combined silicon chip and epoxy/copper post stack-up can be thought of as a ‘molded’ die with an effective CTE (in Figure 8), which will be significantly greater than the CTE of the silicon die itself (2.6×10⁻⁶/°C). This results in a significant reduction of the stresses on solder joints. For a copper post WLP, the redistribution layer (RDL) may be incorporated if needed. However, It has been found that the effect of the polymer film in copper post WLP is not as effective as that in BOP structures [12]. This indicates that for the copper post WLP structure, the dominant effect to reduce the solder joint stresses is due to the larger CTE of copper and epoxy. The modulus of copper/epoxy and the appearance of the RDL (polymer film) are of the secondary effect in solder joint reliability improvement.

![Figure 8 Effective CTE increase of the ‘molded die’ in copper post WLP](image)

Figure 8 Effective CTE increase of the ‘molded die’ in copper post WLP

As opposed to a conventional fan-in WLP, fan-out WLPs start with the reconstitution or reconfiguration of single dies to an artificial molded wafer. The fan-out WLP has received increased attention because of the demand for thinner features and increasing I/O count devices. The reconfigured wafer or fan-out solution provides several advantages:

- Reduced package thickness,
- Fan-out capability (for the increased number of I/O),
- Improved electrical performance,
- Good thermal performance, and
- A substrate-less process.

![Figure 9 Nano-size column-like or honeycomb-like interconnects to replace solder balls](image)

Figure 9 Nano-size column-like or honeycomb-like interconnects to replace solder balls

Another option is the use of polymer-cored solder balls. A plastic core solder ball consists of a large polymer core coated by a copper layer and covered with eutectic and/or lead-free solder. The main advantages of such a system are higher reliability due to the relaxing of stress by the polymer core and a defined ball height after reflow [18]. These balls could improve the solder ball reliability significantly due to the compliant feature of balls. Figure 10 is a schematic of horizontal view of polymer core ball.

![Figure 10 Cross-section structure of polymer core ball](image)

Figure 10 Cross-section structure of polymer core ball

A hollowed solder ball structure, which has the exact same geometry of a regular solder ball, is also proposed [17]. Table 1 shows the results of the inelastic strain energy density and von Mises stress for three ball structures, including regular solder ball, polymer-cored ball, and hollowed solder ball. The displayed results are for the outermost ball in the diagonal direction. Both the maximum and the averaged results are obtained. Table 1 clearly shows the significant reduction in both inelastic strain energy density and stress in solder balls when
A hollow structure is applied. Hollowed ball structures increase the compliance of the WLP during thermal cycling, and thus, less stresses are exerted on the solder ball interface with copper post. On the other hand, it is observed that for polymer-cored solder balls, complicated results are obtained. Maximum stress in polymer-cored solder balls does not show much reduction, especially after the averaged process is done. This indicates that for polymer-cored ball structures, stress distribution is more ‘uniform’ than regular balls. Such results are also confirmed from inelastic strain energy density. The averaged inelastic strain energy density for polymer-cored balls is almost same with the regular balls when the same height is used. In actual applications, the ball height is much less for the regular balls, which will reduce the thermal cycling performance.

Table 1 Comparison of the inelastic strain energy density and von Mises stress for three cases

<table>
<thead>
<tr>
<th>Ball structures</th>
<th>Regular</th>
<th>Polymer-cored</th>
<th>Hollowed</th>
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<tbody>
<tr>
<td>Ball Height (μm)</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Max von Mises Stress</td>
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<td>Stress (MPa)</td>
<td>3.20</td>
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<td>30.72</td>
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<td>Avg. Plastic Work</td>
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6. Summary
This paper presents an overview of wafer level packaging and integration of solid state lighting (SSL) systems. A full realization of wafer level SSL system integration requires wafer level phosphor coating, wafer level LED chip encapsulation, wafer level optics manufacturing, application of through silicon vias (TSV) between LED and silicon/ceramics/polymer wafers, application of wafer-to-wafer or wafer-to-chip bonding and stacking, and the adoption of wafer level bumping technologies. Reconfiguration (or reconstitution) of LED/silicon wafers is also required. A variety of wafer level bumping technologies, such as ball on I/O (BON), ball on polymer (BOP), redistribution dielectric layer (RDL) process, and copper post bumping process, needs to be adopted. The reliability of such a SSL systems is of concern, and newly developed polymer-core interconnect technology and nano-column interconnect will be helpful.

References